REMARKS/ARGUMENT

Claims 1 through 17 are pending. All of the claims are independent except for claim 9. Applicant notes with appreciation the allowance of claims 1-6 and 8-17.

In the Office Action, Claim 7 was rejected under 35 U.S.C. § 102(e) over U.S. Patent No. 6,018,552 ("Uesugi"). Applicant submits that claim 7 is patentable over Uesugi for at least the following reasons.

Claim 7 is directed to a level adjusting circuit that includes: a plurality of bit shifters that shift input baseband signals to the right by different certain bits, a plurality of switches for selecting outputs from said respective bit shifters in accordance with a desired gain desired to be set, and an adder for adding outputs from said respective switches for output as one signal.

In the Office Action, the Examiner took the position that Uesugi's Figure 16 shows the recited bit shifters, in that it shows, at col. 12, lines 57-64, shifters 163, 164 and 168. However, as was pointed out in the previous response, Uesugi does not, among other things, teach the recited plurality of switches for selecting outputs from the respective bit shifters in accordance with a desired gain.

The position was taken in the Office Action that Uesugi's inventing circuit 43 inherently utilizes a plurality of switches to select outputs from the bit shifters with respect to the desired gain. However, to utilize the principle of inherency in an anticipation rejection, the characteristic deemed inherent must *necessarily* follow from the disclosure actually present in the cited reference. In this case, the Examiner has presented no reasoning to support the position that the inventing circuit *must* use a plurality of switches, still less that those hypothetical switches select outputs from the respective bit shifters in accordance with a gain desired to be set.

In fact, it is believed clear from an examination of Figure 16 that the inventing circuit 43 cannot possibly meet or inherently include the switches as those switches are recited in claim 7. As can be seen from that figure, element 43 cannot select outputs from the various bit shifters shown in Figure 16 at least because *it does not have access to the outputs of any of the bit shifters.* Thus, whether or not there may be switches in element 43 is immaterial, since such switches cannot possibly perform the recited function. For at least this reason, no prima facie case of anticipation has been set forth with regard to claim 7.

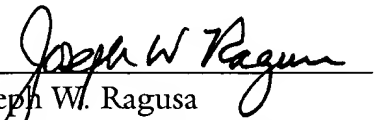
Also, the output of the inventing circuit 43 feeds into an adder that does not add outputs from the switches that are imagined in the Office Action to reside somewhere inside inventing circuit 43. It is clear that the adding circuit 37 adds A, B and C, only B of which originates from the inventing circuit. Claim 7 requires an adder that adds outputs from the respective switches for output as one signal. The adder 37 clearly does not perform this function. In any event, as mentioned in the previous paragraph, any switches that may be resident in element 43, cannot select outputs from the bit shifters.

To summarize the points made in the foregoing paragraphs: (1) there is no teaching of switches being located in the inventing circuit 43; (2) no evidence has been presented in the Office Action to support any inherency argument regarding the presence of hypothetical switches being resident in the inventing circuit 43; (3) even if, for the purposes of argument, it is presumed that some type of switches are resident inside of the inventing circuit 43, they cannot possibly perform the function of the switches recited in claim 7, for the reasons set forth above; and (4) the adding circuit of Uesugi does not interact with the inventing circuit (and the hypothetical switches alleged in the Office Action to inherently reside in the inventing circuit) in the manner in which the adder of claim 7 interacts with the switches of that claim. For at least the above, reasons, no prima facie case of anticipation has been set forth with regard to claim 7.

In view of the foregoing remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Dated: June 16, 2005

Respectfully submitted,

By 

Joseph W. Ragusa
Registration No.: 38,586
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
(212) 835-1400
Attorney for Applicant